

REMARKS

Claim rejection under 35 USC 112

Claim 10 has been rejected under 35 USC 112, second paragraph. In particular, claim 10 recites the limitation “the interrupt-assignment software,” for which there is no antecedent basis. Applicant without prejudice has amended this limitation to instead read “the interrupt-assignor,” for which there is antecedent basis within base independent claim 7. Applicant therefore requests the withdrawal of this rejection.

Claim rejections under 35 USC 103

Claims 1-10, 12-19, and 21-30 have been rejected under 35 USC 103(a) as being unpatentable over Kiick (2003/0200250) in view of “what is well known in the art,” as evidenced by Neal (6,347,349) and Carpenter (6,148,361). The Examiner has stated that Kiick teaches all the limitations of the claimed invention, except that it “fails to teach where one or more of the nodes are processorless and memoryless.” (Office action, p. 4) The Examiner has further stated that he “takes official notice that it is well known in this art to have nodes in NUMA systems that are memoryless and processorless, as evidence by Neal . . . and Carpenter.” (Id.)

Applicant submits, however, that the Examiner has failed to establish proper *prima facie* obviousness of the claimed invention over Kiick in view of “what is well known in the art,” as evidence by Neal and Carpenter, for four different, separate, and independent reasons, each of which is now discussed in detail.

(1) No motivation to modify Kiick to include memoryless and processorless nodes

The Examiner has located all the aspects of the claimed invention within Kiick, except for the memoryless and processorless nodes of the claimed invention. The Examiner has instead stated that having memoryless and processorless nodes “is well known in the art.” However, the “fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not

sufficient by itself to establish *prima facie* obviousness.” (MPEP sec. 2143.01.IV.) More specifically,

A statement that modifications of the prior art to meet the claimed invention would have been “well within the ordinary skill of the art at the time the claimed invention was made” because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references.

(Id., citing Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); see also In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000)) Here, the Examiner has not provided any objective reason to modify Kiick to include processorless and memoryless nodes. Therefore, there is no *prima facie* obviousness of the claimed invention for this reason alone.

(2) Fact that Kiick can be modified does not establish obviousness

As noted above, the Examiner has located all the aspects of the claimed invention within Kiick, except for the memoryless and processorless nodes of the claimed invention. The Examiner has instead stated that having memoryless and processorless nodes “is well known in the art.” However, the “fact that references can be . . . modified is not sufficient to establish *prima facie* obviousness.” (MPEP sec. 2143.01.III.) More specifically, the “mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.” (Id., citing In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Here, the Examiner has not shown how the prior art suggests the desirability to modify Kiick to include processorless and memoryless nodes. Therefore, there is no *prima facie* obviousness of the claimed invention for this reason alone as well.

(3) Provided evidence does not show memoryless and processorless nodes

As noted above, the Examiner has located all the aspects of the claimed invention within Kiick, except for the memoryless and processorless nodes of the claimed invention. The Examiner has instead stated that having memoryless and processorless nodes “is well known in the art,” specifically relying upon Neal and Carpenter as showing such memoryless and processorless nodes. However, Neal and Carpenter do *not* show memoryless and processorless nodes. As such, modifying Kiick in view of Neal and/or Carpenter does not realize the claimed invention, such that the claimed invention is not obvious over Neal and Carpenter.

With respect to Neal in particular, the Examiner has relied upon FIG. 1, item 122; column 1, lines 60-66; and column 3, lines 1-3 thereof as teaching a memoryless and processorless node. However, item 122 refers to a “fabric bridge,” which is specifically *not* an actual node in Neal. Rather, the “fabric bridge is operable for mediating transactions *between nodes* in the data processing system.” (Col. 1, ll. 62-63) “The nodes in . . . a . . . system are coupled via a device, referred to as a ‘fabric,’ which mediates the transactions therebetween.” (Col. 1, ll. 40-43) More specifically, with respect to FIG. 1 in particular, this figure illustrates “a multi-node data processing system 100 [in which] *each node 102* includes a plurality, N, of CPUs 104.” (Col. 3, ll. 21-25) That is, reference number 122 is not a node, but rather reference number 102 is a node – and reference number 122 includes processors 104. Thus, “nodes 102 are coupled via fabric 120,” where “fabric 120 includes fabric bridges 122.” (Col. 3, ll. 43-45)

Thus, what Neal discloses is that you have nodes 102, which have processors 104, and which are coupled to one another via a fabric having a fabric bridge 122. The fabric bridge 122 is not a node, but rather is part of the fabric, which is the device that connects the nodes 102 together. Therefore, in the first instance, Neal’s fabric bridge 122 is not a processorless and memoryless node, such that Kiick in view of Neal does not teach all the limitations of the claimed invention.

Furthermore, even if Neal's fabric bridge 122 were a node, there is no recitation within Neal that the bridge 122 is both memoryless and processorless. In fact, the opposite seems to be true to at least some extent. FIG. 2A of Neal, for instance, shows the fabric bridge 122 in detail, which includes logic 204 and a state machine 206, either of which may be considered a processor, and buffers 202, which may be considered memory. Therefore, the Examiner has to show that the logic 204 and the state machine 206 are not processors, and that the buffers 202 are not memory, for the fabric bridge 122 to be memoryless and processorless. For this reason as well, Kiick in view of Neal does not teach all the limitations of the claimed invention.

With respect to Carpenter in particular, the Examiner has relied upon FIG. 1, item 8 and column 12, lines 16-34 thereof as teaching a memoryless and processorless node. The node 8 of Carpenter is indeed processorless, as it is described as "one or more nodes 8 containing no processors 8." However, the nodes 8 of Carpenter are *not* described as *also* being memoryless. The claimed invention is limited to one or more nodes that are *both* memoryless and processorless. Therefore, because Carpenter's node 8 is not a memoryless node, Kiick in view of Carpenter does not teach all the limitations of the claimed invention.

Because Carpenter and Kick fail to teach memoryless and processorless nodes, the claimed invention is not unpatentable for this reason as well.

(4) Improper Official Notice taken

As noted above, the Examiner has located all the aspects of the claimed invention within Kiick, except for the memoryless and processorless nodes of the claimed invention. The Examiner has instead stated that having memoryless and processorless nodes "is well known in the art," and has taken Official Notice of this fact. Curiously, however, the Examiner also specifically relies upon Neal and Carpenter as showing such memoryless and processorless nodes (which they do not, as has been described above).

To this extent, Official Notice has been improperly taken by the Examiner. The whole point of taking Official Notice is to rely on common knowledge within the art, or well known prior art, *without* and *unsupported by* documentary evidence. (See MPEP, sec. 2144.03) Here, however, the Examiner has *both* taken Official Notice *and* provided references that the Examiner has stated show the common knowledge for which the Examiner has taken Official Notice. That is, there is no need for the Examiner to take Official Notice, since he has already provided references that supposedly document the common knowledge that is the subject matter of the Official Notice.

Therefore, Applicant responds to this Official Notice as follows. First, Applicant challenges the factual assertion that memoryless and processorless nodes are common knowledge, such that the Examiner must support this finding with adequate evidence. (See MPEP, sec. 2144.03.C.) Specifically, Applicant alleges that memoryless and processorless nodes are not common knowledge, as used in the claimed invention. However, the Examiner appears to have already attempted to do this by his reference of Carpenter and Neal. Therefore, second, Applicant refutes that Carpenter or Neal provides adequate documentary support for memoryless and processorless nodes, as discussed in the previous section of this response.

For this reason as well, the claimed invention is not unpatentable.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicant's representative, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Date

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